FIG. 1

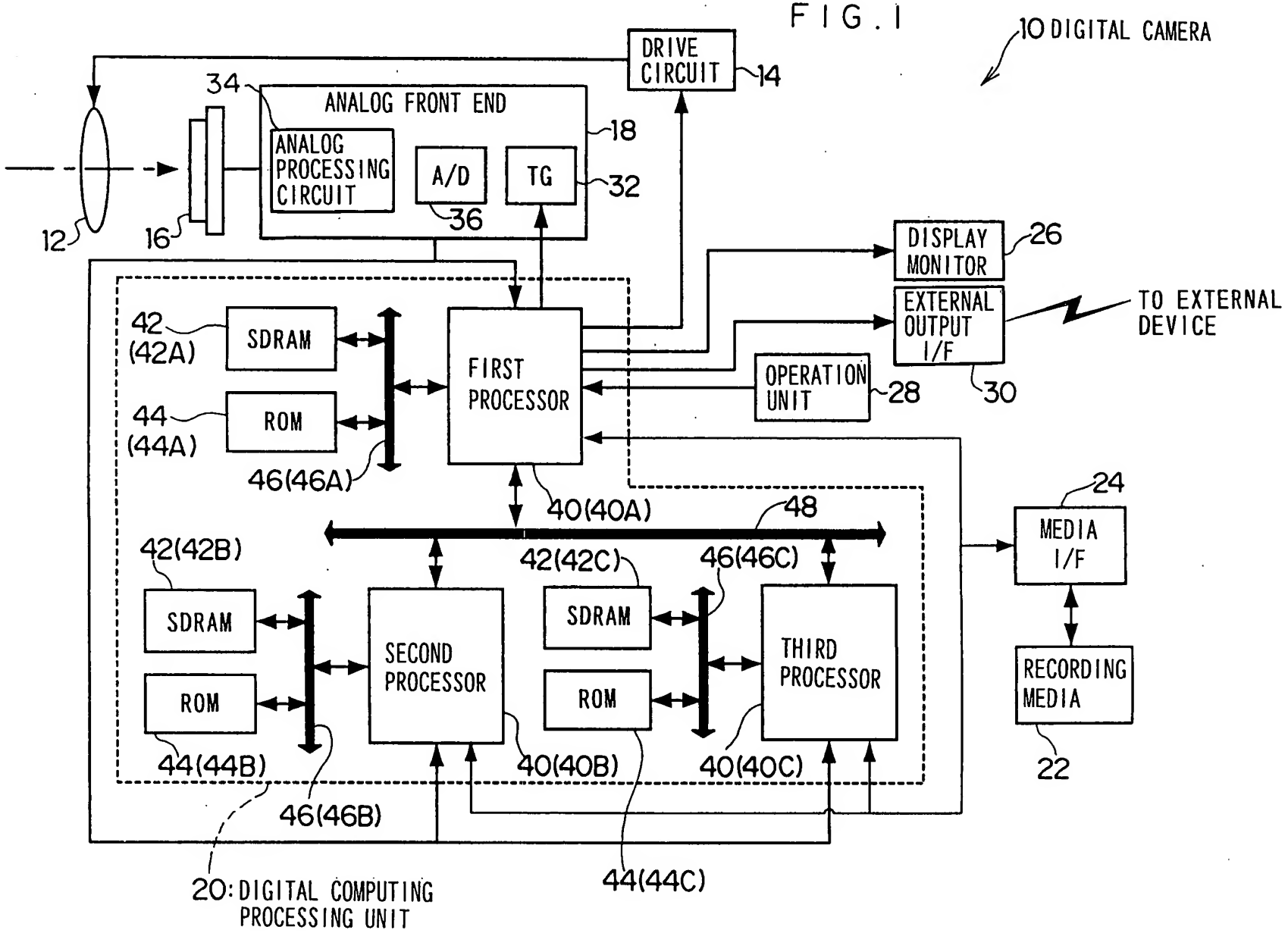

10 DIGITAL CAMERA
DRIVE CIRCUIT
14
34
ANALOG FRONT END
18
ANALOG PROCESSING CIRCUIT
A/D
TG
32
36
12
16
DISPLAY MONITOR
26
EXTERNAL OUTPUT I/F
TO EXTERNAL DEVICE
30
OPERATION UNIT
28
42 (42A)
SDRAM
44 (44A)
ROM
46(46A)
FIRST PROCESSOR
40(40A)
48
24
MEDIA I/F
42(42B)
42(42C)
46(46C)
SDRAM
SDRAM
SECOND PROCESSOR
THIRD PROCESSOR
ROM
ROM
RECORDING MEDIA
44(44B)
40(40B)
40(40C)
22
46(46B)
20: DIGITAL COMPUTING PROCESSING UNIT
44(44C)

FIG. 2

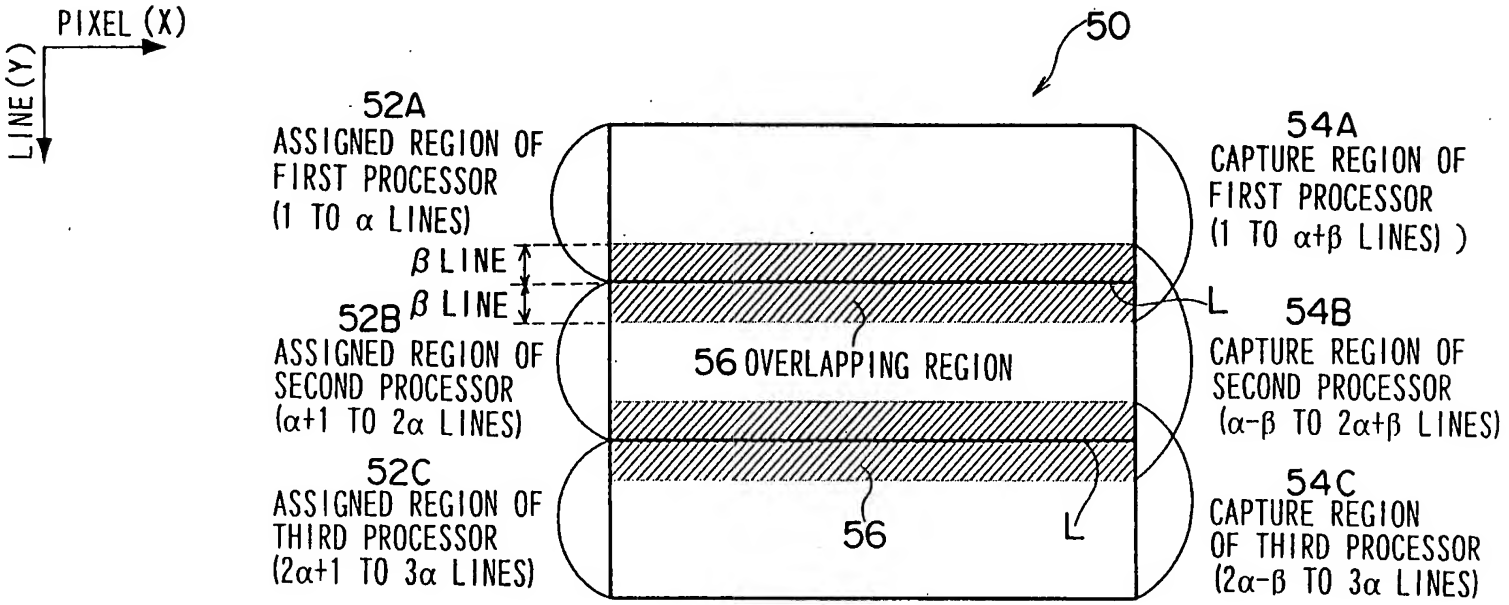

PIXEL (X)
LINE (Y)
50
52A
ASSIGNED REGION OF FIRST PROCESSOR (1 TO α LINES)
β LINE
β LINE
52B
ASSIGNED REGION OF SECOND PROCESSOR (α+1 TO 2α LINES)
52C
ASSIGNED REGION OF THIRD PROCESSOR (2α+1 TO 3α LINES)
56 OVERLAPPING REGION
56
L
L
54A
CAPTURE REGION OF FIRST PROCESSOR (1 TO α+β LINES))
54B
CAPTURE REGION OF SECOND PROCESSOR (α-β TO 2α+β LINES)
54C
CAPTURE REGION OF THIRD PROCESSOR (2α-β TO 3α LINES)

FIG. 3A

−1	−1	−1
−1	9	−1
−1	−1	−1

FIG. 3B

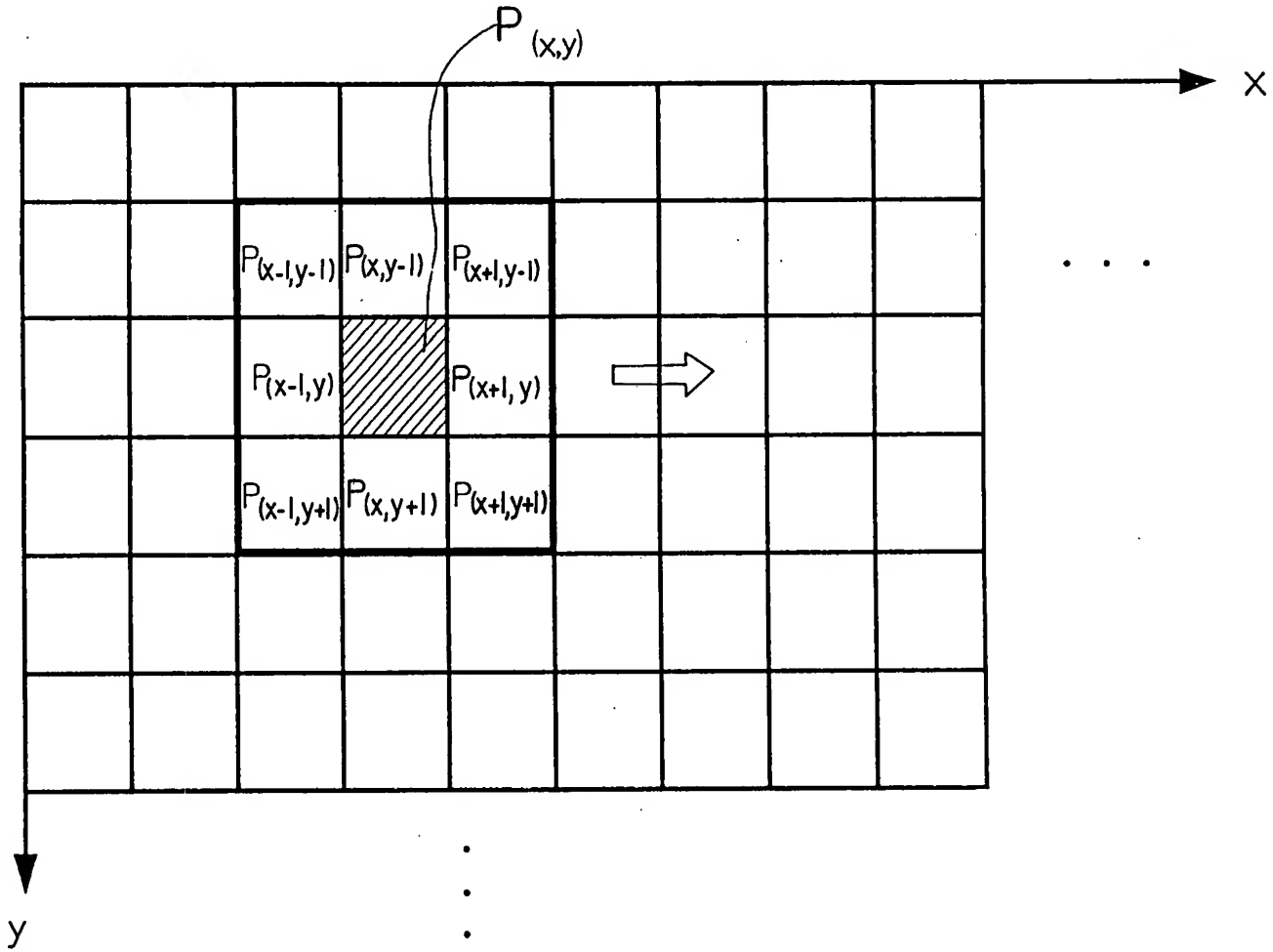


FIG. 4

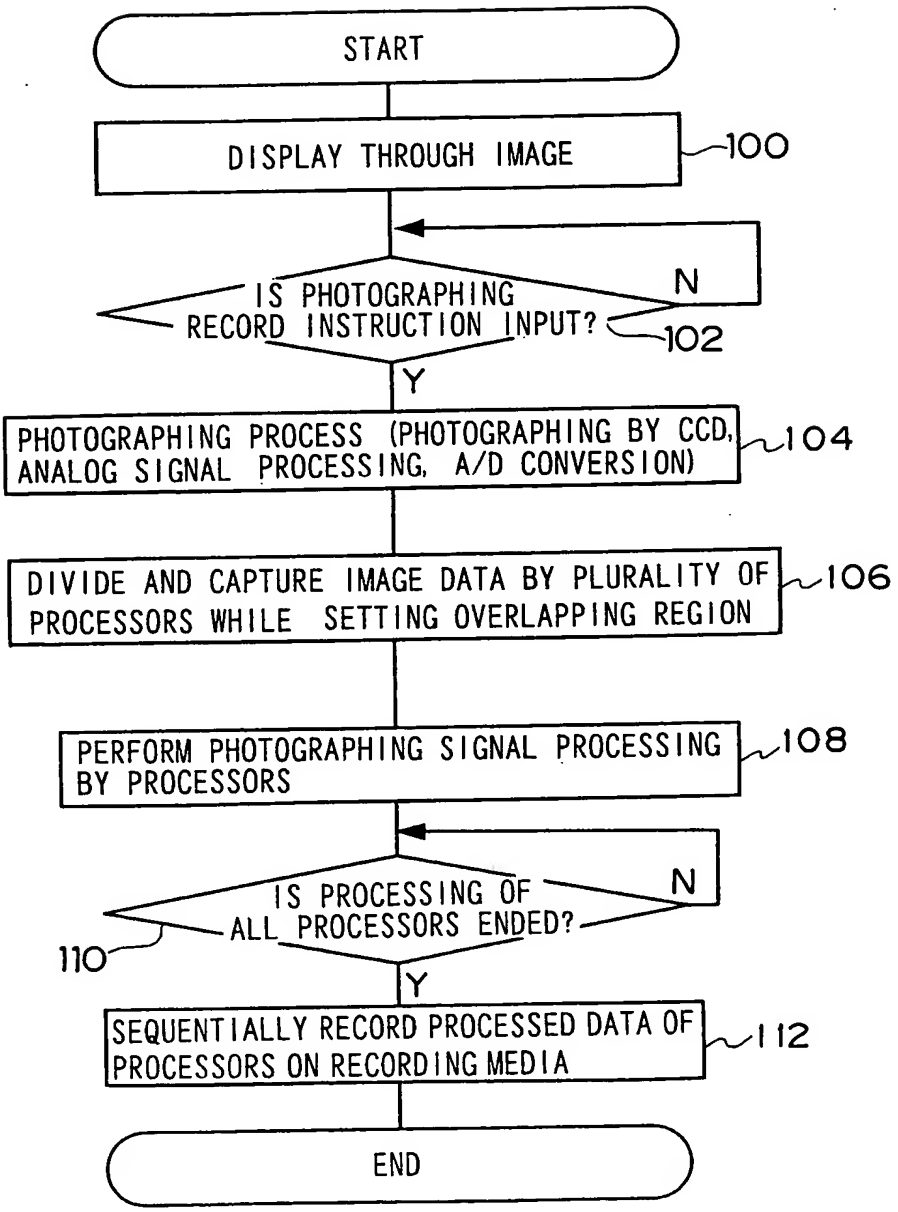

START
DISPLAY THROUGH IMAGE
100
IS PHOTOGRAPHING RECORD INSTRUCTION INPUT?
N
102
Y
PHOTOGRAPHING PROCESS (PHOTOGRAPHING BY CCD, ANALOG SIGNAL PROCESSING, A/D CONVERSION)
104
DIVIDE AND CAPTURE IMAGE DATA BY PLURALITY OF PROCESSORS WHILE SETTING OVERLAPPING REGION
106
PERFORM PHOTOGRAPHING SIGNAL PROCESSING BY PROCESSORS
108
IS PROCESSING OF ALL PROCESSORS ENDED?
N
110
Y
SEQUENTIALLY RECORD PROCESSED DATA OF PROCESSORS ON RECORDING MEDIA
112
END

FIG. 5

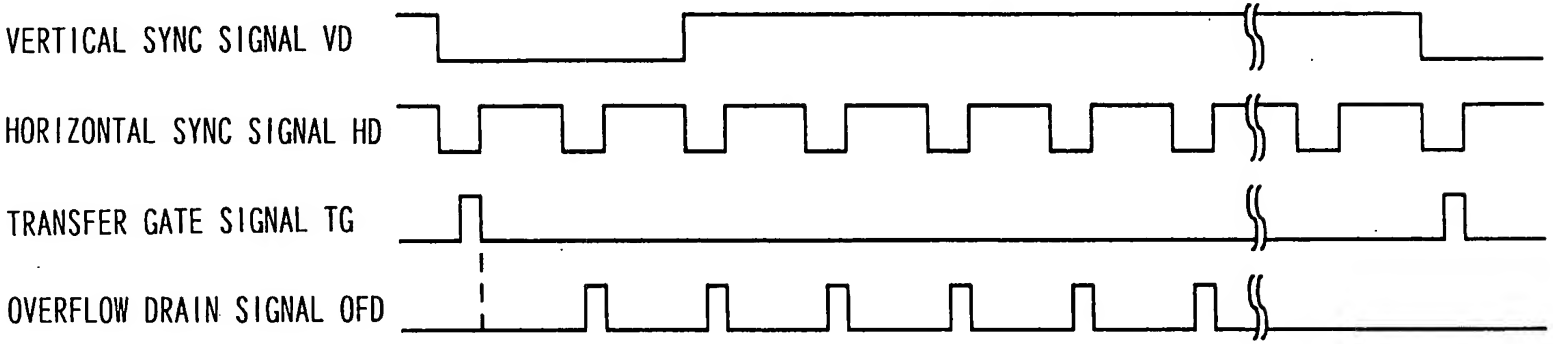

VERTICAL SYNC SIGNAL VD
HORIZONTAL SYNC SIGNAL HD
TRANSFER GATE SIGNAL TG
OVERFLOW DRAIN SIGNAL OFD

FIG. 6

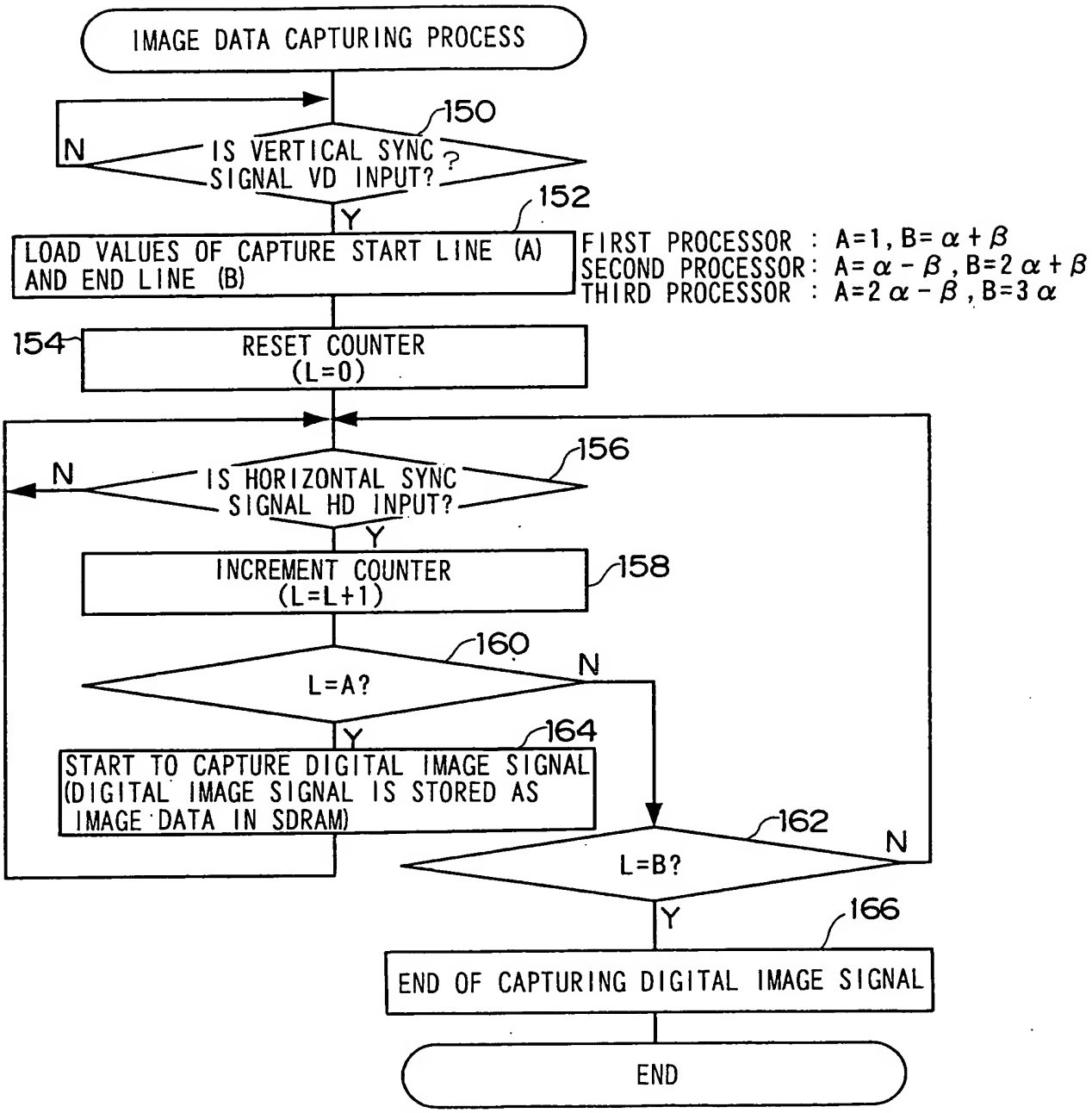


IMAGE DATA CAPTURING PROCESS
150
N
IS VERTICAL SYNC SIGNAL VD INPUT?
Y
152
LOAD VALUES OF CAPTURE START LINE (A) AND END LINE (B)
FIRST PROCESSOR : A=1, B=α+β
SECOND PROCESSOR: A=α-β, B=2α+β
THIRD PROCESSOR : A=2α-β, B=3α
154
RESET COUNTER (L=0)
156
N
IS HORIZONTAL SYNC SIGNAL HD INPUT?
Y
INCREMENT COUNTER (L=L+1)
158
160
L=A?
N
Y
164
START TO CAPTURE DIGITAL IMAGE SIGNAL (DIGITAL IMAGE SIGNAL IS STORED AS IMAGE DATA IN SDRAM)
162
L=B?
N
Y
166
END OF CAPTURING DIGITAL IMAGE SIGNAL
END

FIG. 7A

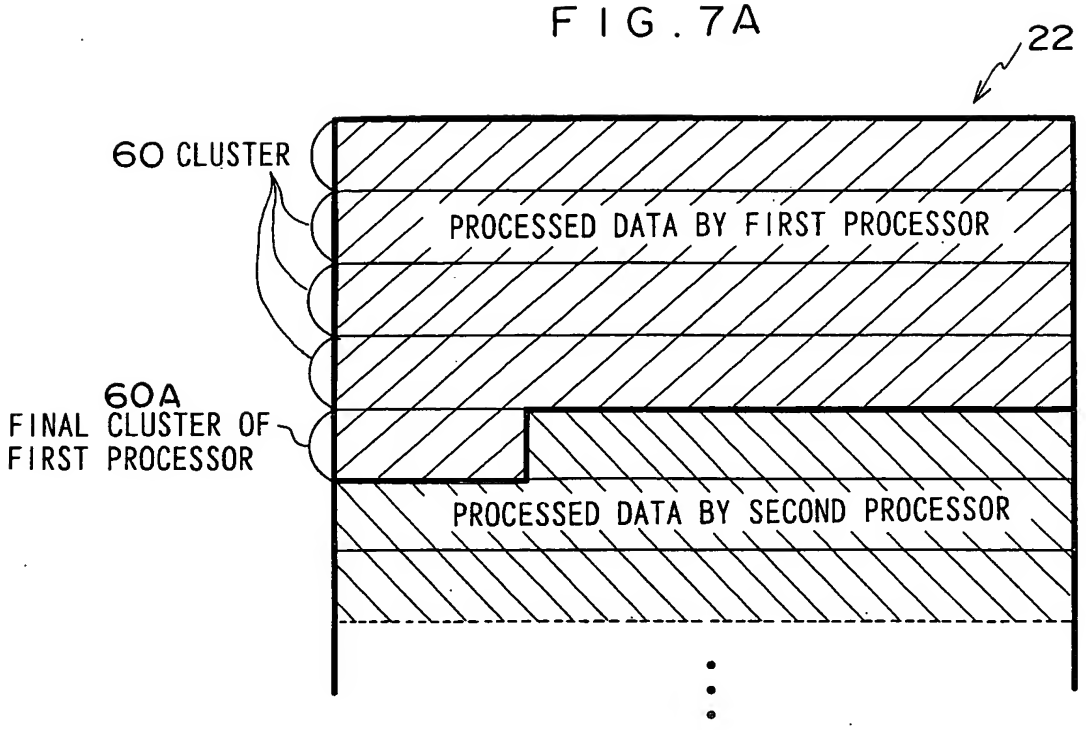

22
60 CLUSTER
PROCESSED DATA BY FIRST PROCESSOR
60A
FINAL CLUSTER OF
FIRST PROCESSOR
PROCESSED DATA BY SECOND PROCESSOR

FIG. 7B

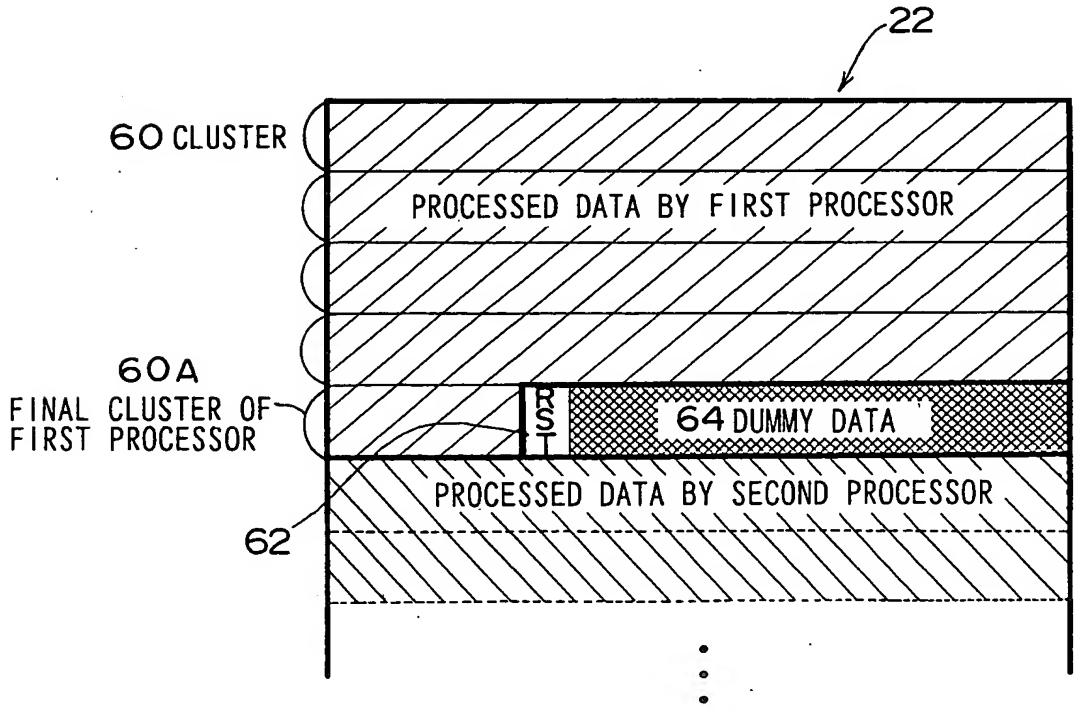

22
60 CLUSTER
PROCESSED DATA BY FIRST PROCESSOR
60A
FINAL CLUSTER OF
FIRST PROCESSOR
RST
64 DUMMY DATA
PROCESSED DATA BY SECOND PROCESSOR
62

FIG. 8A

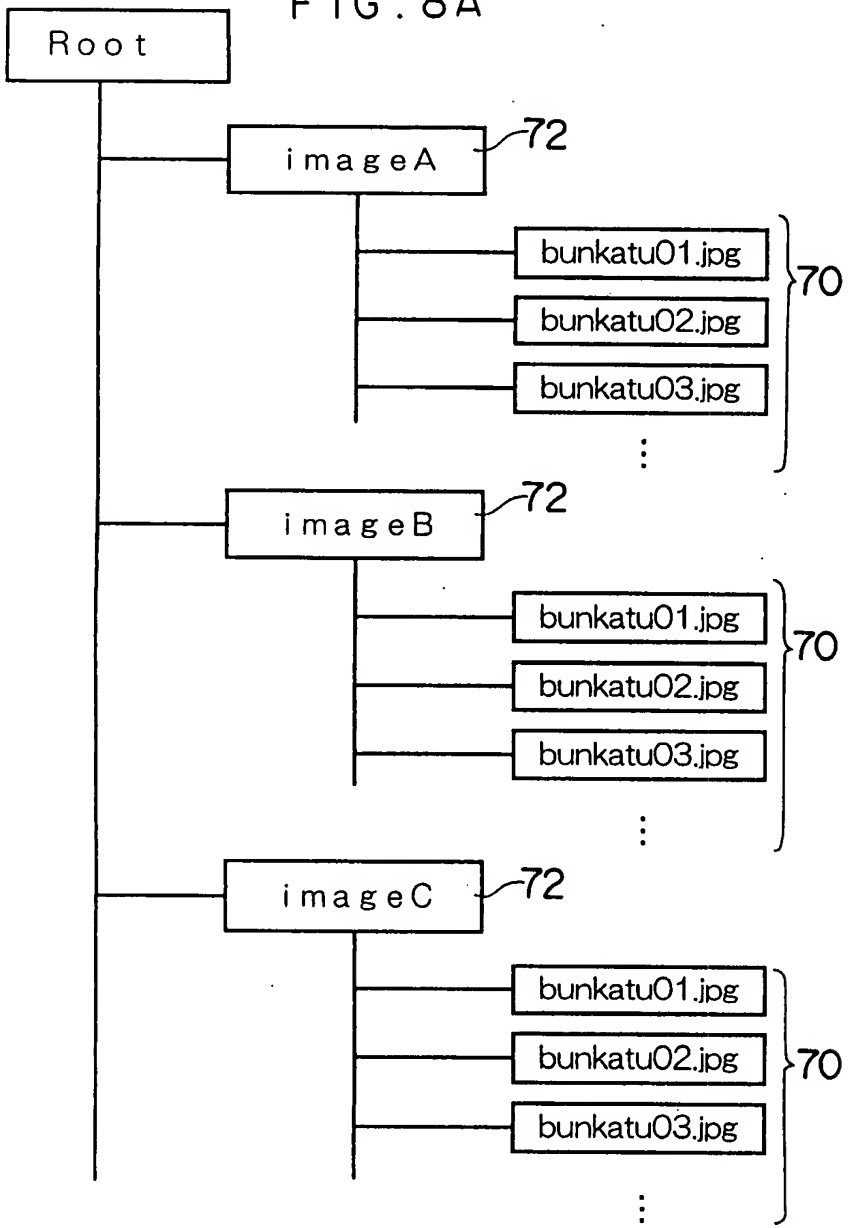
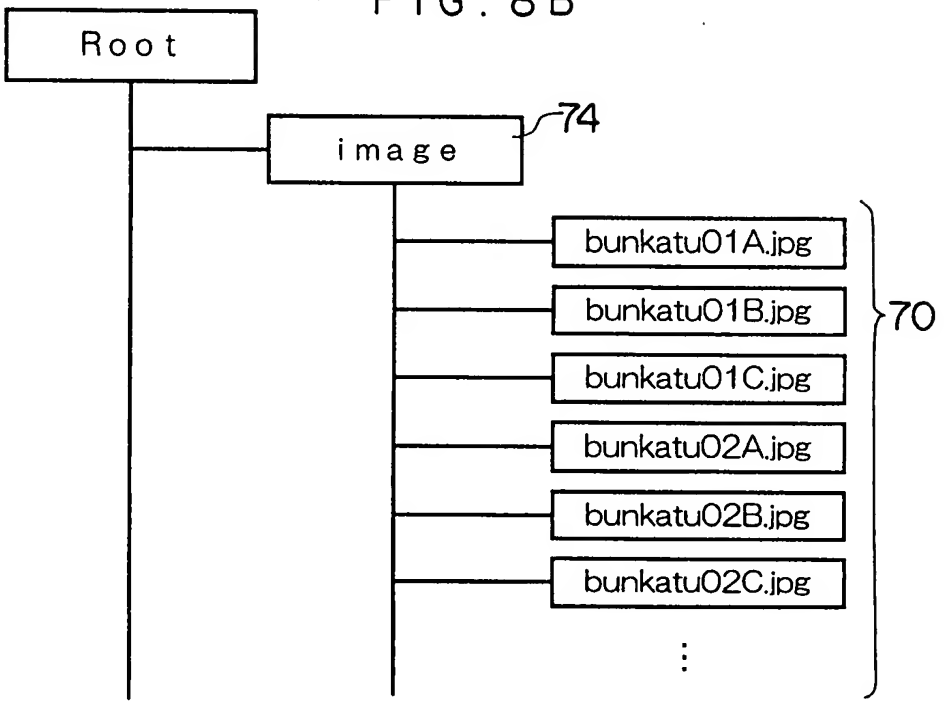

Root
imageA
72
bunkatu01.jpg
bunkatu02.jpg
bunkatu03.jpg
70
imageB
72
bunkatu01.jpg
bunkatu02.jpg
bunkatu03.jpg
70
imageC
72
bunkatu01.jpg
bunkatu02.jpg
bunkatu03.jpg
70

FIG. 8B


Root
image
74
bunkatu01A.jpg
bunkatu01B.jpg
bunkatu01C.jpg
bunkatu02A.jpg
bunkatu02B.jpg
bunkatu02C.jpg
70